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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,832	07/21/2003	Steven P. Young	X-1335 US	6570

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary	Application No.	Applicant(s)	
	10/624,832	YOUNG, STEVEN P.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,20,21 and 23-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *35 and 36* is/are allowed.

6)☒ Claim(s) *1-5,7-9,11-17,21 and 23-34* is/are rejected.

7)☒ Claim(s) *6,10,18 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/27/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 23-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Mohsen (5,432,708).

Claim 23, Mohsen shows a system (80, Fig. 3) having a plurality of dice (I.C.), comprising:

a first die (10a, Fig. 3) of the plurality of dice comprising a first plurality of columns (two columns, Fig. 1), each column of the first plurality of columns having a first plurality of substantially identical elements (12a-12d, Fig. 1);

a second die (10c, Fig. 3) of the plurality of dice comprising a second plurality of columns (two columns, Fig. 1), each column of the second plurality of columns having a second plurality of substantially identical elements (12a-12d, Fig. 1); and

a plurality of signal lines (86a, col. 5, lines 25-26) connecting each element of the first plurality of substantially identical elements of each column of the first plurality of columns with an associated element of the second plurality of substantially identical elements of an associated column of the second plurality of columns (col. 25-30).

Claim 24, Mohsen shows the system of claim 23 wherein a particular column of the first plurality of columns and the particular column's associated column form an

aggregated column of the device (this is inherent limitation since column from IC 10a connected to column from 10c by internal pads 62 and signal lines 86a).

Claim 25, Mohsen shows the system of claim 23 wherein the plurality of signal lines include greater than 100 lines (few hundreds to few thousand, col. 6, lines 1-2).

Claim 26, Mohsen shows the system of claim 23 wherein the plurality of signal lines include greater than 1000 lines (few hundreds to few thousand, col. 6, lines 1-2).

Claim 27, Mohsen shows the system of claim 23 further comprising a carrier die (82, Fig. 3) having the plurality of signal lines.

Claim 28, Mohsen shows the system of claim 23 wherein each column of the first plurality of columns (10a, Fig. 3) is filled with the first plurality of substantially identical elements (12a-12d, Fig. 1), and each column of the second plurality of columns (10c, Fig. 3) is filled with the second plurality of substantially identical elements (12a-12d, Fig. 1).

Claim 29, Mohsen shows a system having a plurality of dice (I.C., Fig. 3), the system comprising:

a first die (10a, Fig. 3) of the plurality of dice, comprising all input/output blocks (76, Fig. 1) on the first die for communicating with circuits located outside of the first die, and a first function block (12a-12b, Fig. 1) connected to a first interconnect line (64a and 64b, Fig. 1);

a second die (10a, Fig. 3) of the plurality of dice, comprising second input/output blocks (76, Fig. 1) for communicating with circuits located outside of the second die,

and a second function block (12a-12b, Fig. 1) connected to a second interconnect line (64a and 64b, Fig. 1); and

a signal line (86a, Fig. 3) connecting the first interconnect line to the second interconnect line, wherein a signal propagates from the first interconnect line to the second interconnect line without propagating through any of the input/output blocks of the first die (62a-62y are internal pads which are directly connect to another 62a-62y I.C., col. 5, lines 25-30).

Claim 30, Mohsen shows the system of claim 29 wherein the signal does not propagate through any of the second input/output blocks of the second die.

Claim 31, Mohsen shows the system of claim 29 wherein the first function block is connected to the second function block via the signal line (62a-62y are internal pads which are directly connect to another 62a-62y I.C., col. 5, lines 25-30).

Claim 32, Mohsen shows the system of claim 29 further comprising a carrier die (82, Fig. 3) plurality of dice upon which the first die and second die are mounted, wherein the carrier die comprises the signal line (86a).

Claim 33, Mohsen shows the system of claim 29 wherein the first function block and the second function block are configurable logic blocks (col. 3, lines 20-21).

Claim 34, Mohsen shows the system of claim 29 wherein the first function block an application specific circuit (ASIC, col. 1, lines 67 and col. 3, lines 21-25 teaches any circuits are adaptable for MCM use).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7-9, 11-17, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mohsen (5,654,561).

Claim 1, Mohsen shows a multi-chip device (80, Fig. 3) comprising:

each region (portion of an array circuit of Fig. 1, e.g. two rows and two column as one region as indicated by 10) having a programmable interconnection (70, 60, 58, Fig. 1);

a first Integrated Circuit (10a, Fig. 3) having a first region (10, Fig. 1);

a second IC (10c, Fig. 3) having a second region (10, Fig. 1); and

a supporting structure (82) having one or more signal lines (86a, col. 5, lines 25-26), wherein the first region is directly connected to the second region via one of the signal lines (a plurality of lines connecting together a selected number of I/O pads 62a-62y of one individual high I/O count integrated circuit to a selected number of I/O pads 62a-62y of another high I/O count integrated circuit, col. 5, lines 25-30), wherein a circuit in the first region is connected to a circuit in the second region without use of any input/output (I/O) bank on the first IC (I/O pads 62a-62y are internal pads **not** input/output bank, 76 & 74, see figure 2).

Mohsen discloses the claimed invention except for aligning the first region and the second region and connecting them. It would have been obvious to one having ordinary skill in the art at the time the invention was made to align the first region in the first integrated circuit (10a, Fig. 3) with the second region in the second integrated circuit (10c, Fig. 3) and connecting them together, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

Claim 2, Mohsen shows the multi-chip device of claim 1 wherein the supporting structure comprises a carrier die (MCM substrate, col. 4, line 66).

Claim 3, Mohsen shows the multi-chip device of claim 1 wherein each region further comprises programmable logic (PPGA, col. 3, lines19-21).

Claims 4 and 5, Mohsen discloses the claimed invention except for the group of the aligned regions on the first IC and the second IC is substantially identical. It would have been an obvious to one having ordinary skill in the art at the time the invention was made to have the regions of the first IC and the second IC identical since it was known in the art the multi-chip device included identical chips and different chips in order to provide various applications on single chip.

Claim 7, Mohsen shows the multi-chip device of claim 1 wherein the second region includes a tile (12a-12d) of a field programmable gate array.

Claim 8, Mohsen shows a multi-chip module having:

a first die (10a, Fig. 3) having a first column (e.g. two column in 10 of Fig. 1) of a first plurality of tiles (12a-12d), wherein each tile of the first plurality includes programmable logic (col. 3, lines 20-21);

a second die (10c, Fig. 3) having a second column (e.g. two column in 10 Fig. 1) of a second plurality of tiles (12a-12d); and

a supporting substrate (82) having a plurality of signal lines, wherein a tile in the first column is directly connected to a tile in the second column via one of the plurality of signal lines (a plurality of lines connecting together a selected number of I/O pads 62a-62y of one individual high I/O count integrated circuit to a selected number of I/O pads 62a-62y of another high I/O count integrated circuit, col. 5, lines 25-30) and without using any input/output (I/0) bank on the first die (I/O pads 62a-62y of Fig. 1 are internal pads **not** input/output bank, 76 & 74).

Mohsen discloses the claimed invention except for aligning the first column and the second column and connecting them. It would have been obvious to one having ordinary skill in the art at the time the invention was made to align the first column in the first integrated circuit (10a, Fig. 3) with the second column in the second integrated circuit (10c, Fig. 3) and connecting them together, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

Claim 9, Mohsen shows the multi-chip module of claim 8 wherein the tile in the first column comprises a logic block (12a-12d) and a switching block (a square comprises little circles indicated as 58 in figure 1).

Claim 11, Mohsen shows the multi-chip module of claim 8 wherein the first die includes configuration logic (col. 3, lines 19-21).

Claim 12, Mohsen shows the multi-chip module of claim 8 wherein the first die includes a portion of a programmable logic device (col. 3, lines 19-21).

Claims 13 and 14, Mohsen discloses the claimed invention except for the first die and the second die is substantially identical or heterogeneous. It would have been an obvious to one having ordinary skill in the art at the time the invention was made to have the regions of the first IC and the second IC identical or heterogeneous since it was known in the art the multi-chip device included identical chips and different chips in order to provide various applications on a single chip.

Claims 15-16, Mohsen discloses programmable logic and ASIC circuit are used to build reprogrammable ASIC device (col. 1, lines 66-67) are well known, therefore Mohsen discloses the claimed invention except for the second die has programmable logic and an embedded application specific integrated circuit is selected from a group consisting of a microprocessor, a digital signal processor, and an arithmetic processing module. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the second die has programmable logic and an embedded application specific integrated circuit is selected from a group consisting of a microprocessor, a digital signal processor, and an arithmetic processing module, since it

has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. Howard v. Detroit Stove Works, 150 U.S. 164 (1893).

Claim 21, Mohsen discloses a multi-chip module, having programmable interconnections, comprising;

means (e.g. an array of programmable logic and interconnection, Fig1 and col. 3, lines 13-14) for arranging a first plurality of substantially identical connected regions (each region includes 12a-12d and the interconnection associated with it) on a first integrated circuit (10a, Fig. 3);

means (e.g. an array of programmable logic and interconnection, Fig1) for arranging a second plurality of substantially identical connected regions (each region includes 12a-12d and the interconnection associated with it) on a second IC (10c, Fig. 3); and

means (86a and 82, Fig. 3) for connecting a first region in the first plurality to a second region in the second plurality: and

Mohsen further discloses means for directly connecting (an array of internal I/O pads [62, Fig. 2] can be connected to one another [col. 7, lines 56-65]).

Mohsen discloses the claimed invention except for a first region of the first plurality connecting to a second non-adjacent region of the first plurality.
It would have been an obvious matter of design choice to connect a first region of the first plurality to a second non-adjacent region of the first plurality, since Mohsen teaches

that an array of internal I/O pads (62, Fig. 2) can be selected connected to one another as user-definable function circuits (col. 7, lines 56-65).

Allowable Subject Matter

2. Claims 6, 10, 18, and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. Claims 35-36 are allowed.

4. The following is an examiner's statement of reasons for allowance: with respect to claim 35, in addition to other limitations in the claim, the prior art of record fails to teach, disclose or render obvious the applicant's invention as claimed, particularly the feature describing a driver connected to the first interconnect wire, the driver not part of an input/output block.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

11/18/05